

CLAIMS:

1. A wafer (1) which wafer (1) comprises a number of exposure fields (2) and which wafer (1) comprises a number of lattice fields (3) in each exposure field (2), wherein each lattice field (3) contains an IC (4) and each IC (4) contains a plurality of IC components, and which wafer (1) comprises a first group (5) of first saw paths (6) and a second group (7) of second saw paths (8), wherein all of the first saw paths (6) of the first group (5) run

5 parallel to a first direction (X) and have a first path width (W1) and wherein all of the second saw paths (8) of the second group (7) run parallel to a second direction (Y) intersecting the first direction (X) and have a second path width (W2), and wherein the first saw paths (6) and the second saw paths (8) are provided and designed for a subsequent segregation of the lattice fields (3) and the ICs (4) contained therein, and wherein in each exposure field (2) at least

10 two control module fields (A1, A2, B1, B2, C1, C2, D1, D2) are provided, each of which control module fields (A1, A2, B1, B2, C1, C2, D1, D2) runs parallel to the first direction (X) and thus to the first saw paths (6) and contains at least one optical control module (OCM-A1, OCM-A2, OCM-B1, OCM-B2, OCM-C1, OCM-C2, OCM-D1, OCM-D2), wherein each

15 control module (OCM-A1, OCM-A2, OCM-B1, OCM-B2, OCM-C1, OCM-C2, OCM-D1, OCM-D2) contains a plurality of control module components (10, 11, 12, 13, 14, 15, 16, 17, 18), and wherein each control module field (A1, A2, B1, B2, C1, C2, D1, D2) within an exposure field (2) comprises a plurality of control module field sections (A11, A12,

.....A1N and A21, A22,A2N and B11, B12,B1N and B21, B22,

20B2N and C1N and C2N and D1N and D2N) and is distributed among several lattice grids (3), and wherein each control module field section (A11 to D2N) is located in a lattice field (3) and contains at least one control module component (10, 11, 12, 13, 14, 15, 16, 17, 18).

25 2. A wafer (1) as claimed in claim 1, wherein each control module field section (A11 to D2N) in each lattice field (3) is located in the same position, in which position the IC (4) in the lattice field (3) in question does not have any IC components.

3. A wafer (1) as claimed in claim 1, wherein the at least two control module fields (A1, A2, B1, B2, C1, C2, D1, D2) of each exposure field (2) are arranged at an average distance (K) from one another extending in the second direction (Y), which average distance (K) is equal to at least a quarter of the side length (L) of a side (M) of the exposure field (2) which extends in the second direction (Y).

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4. Wafer (1) as claimed in claim 3, wherein the average distance (K) is equal to the whole side length (L) of a side (M) of the exposure field (2), which area extends in the second direction (Y) minus the side length (N) of a side (P) of a lattice field (3) which 10 extends in the second direction (Y).